REMARKS

After entry of this amendment, claims 1-6 and 16-30 will be pending in this application. Claim 1 has been amended. Claims 7-15 have been canceled without prejudice. New claims 22-30 have been added. Support for the new and amended claims can be found in the specification. No new matter has been added.

Claims 1-6 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hoover, United States patent number 4,117,415. Claims 1-6 and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Gabara, United States patent number 5,483,207. Claims 17-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara.

Reconsideration of these rejections and allowance of all the pending claims in light of the included amendments and remarks is respectfully requested.

Formalities

Claim 1 stands rejected under 35 U.S.C. 112 for indefiniteness. This rejection has been obviated by amendment.

Redlined and corrected versions of Figures 1, 2, 3, 8, and 10 have been submitted for the Examiner's approval. Specifically, M1 130 and M2 140 in Figure 1 have been relabeled M10 130 and M20 140 to avoid confusion with M1 410 and M2 420 in Figure 4. Similarly, ID1 and ID2 in Figure 2 have been changed to ID10 and ID20.

C1 355 in Figure 3 has been relabeled C10 355 to avoid confusion with C1 490 in Figure 4. The spelling of the word "proportional" in Figure 8 has been corrected, and the reference identifier 1010 in Figure 10 has been removed.

This amendment will be faxed, and so the drawings will not be redlined when received. Thus, an additional set of marked up drawings are being simultaneously mailed. In order to advance prosecution of this application, applicant requests that the faxed drawings be accepted by the Examiner.

Changes corresponding to the above drawing corrections and amendments to correct typographical errors have been made to the specification.

Claim 1

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Hoover. But Hoover does not teach each and every element of the claim. For example, claim 1, as amended, recites "generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity." Hoover does not provide feature.

Specifically, Figure 2 of Hoover is cited in the office action as teaching each and every element of this claim. (Page 4 of office action dated December 17, 2001). But Hoover describes the four active devices as being operated as Class A amplifiers. (Hoover, column 3, lines 20-26). A Class A amplifier is defined as "an amplifier in which the active device acts as a modulated current source biased midway between saturation and conduction cutoff. In a Class A amplifier, as the amplitude of an applied sinusoidal signal is increased, the output will start to clip at both ends simultaneously..." (Comprehensive Dictionary of Electrical Engineering, IEEE press, 1999).

Class A amplifiers do not generate a first current that is approximately equal to zero when the input signal has a second polarity as required by the claim. Rather, applicants submit that Class A amplifiers generate a first current that is proportional to the input signal when the input signal has a first or a second polarity, so long as clipping is avoided.

Claim 1 provides a method of buffering an input signal that saves power by generating a current that is approximately zero when an input signal has a second polarity. Hoover does not provide this benefit.

Claim 1 also stands rejected under 35 U.S.C. 102(b) as being anticipated by Gabara. But Gabara does not teach each and every element of this claim either. For example, claim 1, as amended, recites "a method of buffering an input signal." Gabara does not buffer input signals.

Figure 2A of Gabara is cited by the office action as teaching each and every element of this claim. (Office action, page 5, second paragraph). But this figure shows an oscillator, not a buffer. Oscillators are circuits that generate periodic signals. Their input signals may include, as does the cited circuit, a control voltage for adjusting the frequency of operation. Oscillators do not buffer input signals. In fact, oscillators are unstable, that is they oscillate between two states, a undesirable condition for a buffer. Accordingly, Gabara teaches away from using the circuit of Figure 2A as a buffer for input signals.

Claim 1 also recites:

> receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity; generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity; generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity.
> (applicant's claim 1, emphasis added).

Devices 30p and 32p in Figure 2A of Gabara are p-channel current sources whose current is set by the control voltage Vpch. (Gabara, column 4, line 3-10). Vpch is a control voltage, it is not a pair of complimentary signals as described in the office action. (Office action, page 6, lines 3 and 4). The currents generated by devices 30p and 32p are thus approximately equal, ignoring channel length modulation effects.

But the claim requires a first current "proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity" and a second current "proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity." Thus, the first and second currents required by the claim are not equal to each other. Accordingly, the first and second currents required by the claim are not generated by the structure disclosed by Gabara.

For at least these reasons, claim 1 should be allowable.

Claim 16

Claim 16 stands rejected under 35 U.S.C. 102(b) as being anticipated by Gabara. But Gabara does not teach each and every element of this claim. For example, claim 16 recites "a first device coupled between a first output node and a first supply node, having a control electrode coupled to a first input node; a second device coupled between a second output node and the first supply node, having a control electrode coupled to a second input node." Gabara does not provide this feature.

Again, Gabara provides an oscillator having one input, which is control input voltage Vpch. Accordingly, Gabara does not provide a second device having a control electrode coupled to a second input as required by the claim.

Also, claim 16 recites "a circuit for buffering RF signals." Figure 2 of Gabara does not provide a circuit for buffering RF signals. Rather, Gabara provides an oscillator, a circuit for generating periodic signals.

For at least these reasons, claim 16 should be allowed.

Other Claims

Claims 2-6 depend on claim 1, and should be allowed for similar reasons as claim 1, and for the additional limitations they recite.

Claims 17-21 depend on claim 16, and should be allowed for similar reasons as claim 16, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Figure 1 is a schematic for a conventional RF buffer 100 used in wireless circuits. Included are differential pair [M1] M10 130 and [M2] M20 140, inductive loads L1 110 and L2 120, and current source 150. Current source 150 provides a bias current for the buffer. A first supply voltage VDD is applied on line 160, and a second supply voltage VSS is applied on line 155. An input voltage Vin between lines 135 and 145 is applied to the gates of devices [M1] M10 130 and [M2] M20 140. This differential input voltage creates a differential current in the drains of the input devices, which appears across the inductive loads, resulting in an output voltage Vout between lines 165 and 170. The terms line and node are used interchangeably throughout this document.

The performance of this RF buffer is limited. Specifically, this circuit has an undesirably high supply current. For example, when the input voltage is at a maximum such that the voltage on line 135 is much higher in the voltage on line 145, devices [M1] M10 130 conducts the current of the current source 150, steering it through load L1 110. This current does not pass through the second load device L2 120, thus the supply current is seen by only one half the differential load L1 110 and L2 120.

When the voltage Vin is near zero, the voltage on line 135 is equal to, or nearly equal to, the voltage on line 145, and the currents in devices [M1] M10 130 and [M2] M20 140 are approximately balanced. At this time, there is no differential current in the drains of the input devices, and the rate of change of current in the loads L1 110 and L2 120 is minimal. Thus, the bias current from current source 150 is wasted, since at this point it does not contribute to the output swing. Furthermore, this circuit has limited output voltage range. Since the loads are inductive, the output lines 165 and 170 swing above and below the supply voltage VDD provided on line 160. But there is a limit to how low an output node can swing. Specifically, if the voltage at line 170 decreases, device [M1] M10 130 enters its triode region, reducing the head room from current source 150, either reducing its output or shutting it off. Accordingly, Vin should be biased to provide sufficient head room for the operation of current source 150, and the

output swing should be limited to avoid driving input devices [M1] M10 130 and [M2] M20 140 into their triode regions.

The drain currents of devices [M1] M10 130 and [M2] M20 140 are shown as waveforms 220 and 230 respectively. Each current is plotted against a Y axis, 222 and 232, corresponding to current amplitude, and an X axis, 224 and 234, corresponding to time. If the input voltage is of sufficient magnitude, then each current waveform has a maximum value of the current in current source 150, ICS, and a minimum value of zero. These two current waveforms are 180 degrees out of phase with each other. The current waveform in [M1] M10 130 is out of phase with the input voltage Vin, while the drain current of [M2] M20 140 is in phase.

Figure 3 is a simplified schematic for an RF buffer amplifier 300 consistent with an embodiment of the present invention. Included are switches S1 310, S2 320, S3 330, and S4 340, inductive load L1 350, and capacitor [C1] C10 355. Inductor L 1 350 and capacitor [C1] C10 355 form a tank circuit. The capacitor [C1] C10 355 may be a real capacitor, it may be the capacitance of the switches plus the capacitance of the interconnect between the inductor and switches, or it may be a combination of the two. A first supply voltage VDD is applied on line 360. A second supply voltage VSS is applied on line 370. In one embodiment of the present invention VDD is equal to 1.8 V and VSS is ground or 0 Volts. Alternately, VDD may be other supply voltages. For example, VDD may be equal to 2.5 or 3.3 Volts. An output voltage is generated across the inductive load L1 350, appearing at lines [385] 380 and 390.

An input signal controls the state of the four switches. When the input has a first polarity, switches S4 340 and S1 310 are closed, and S2 320 and S3 330 are open. Current flows from VDD applied on line 360, through S1 310, through the tank circuit L1 350 and [C1] C10 355, into S4 340, returning to ground or VSS on line 370. When the input has a second polarity, S2 320 and S3 330 are closed while S1 310 and S4 340 are open. In this state current flows from the supply voltage VDD on line 360, through the

switch S2 320, through the tank circuit L1 350 and [C1] C10 355, into switch S3 330, returning to ground or VSS on line 370. The change in current through the tank circuit L1 350 and [C1] C10 355 creates a voltage output between the lines 380 and 390.

Figure 5 is a schematic showing the circuit components in the current path discussed above. Again, as the input voltage increases, the voltage on line 415 increases, and the gate voltage of device M2 420 increases. Device M2 420 conducts an increasing amount of current which flows through cascode device M4 440. This current flows through inductor L1 480. Accordingly, the voltage at line 445 decreases, while the voltage at line at 455 increases. This decreasing voltage at line 445 turns on device M7 470, which conducts current back through inductor L1 480. Again, as the voltage on line 445 continues to decrease, the device M7 4 70 turns on harder, thus increasing the voltage at 455 and decreasing voltage at [455] 445 at an increasing rate.

Figure 6 illustrates the current and voltage waveforms at some of the nodes in the circuit of Figure 4. Input voltage waveform 610 [and] is plotted as a function of time along X axis [640] 614. Input waveform 610 is an example of a signal Vin which may be applied between lines 415 and 425. Input waveform 610 has an average value of zero, a peak voltage of Vinmax, and a minimum voltage of Vinmin. Input waveform 610 is shown as being approximately sinusoidal, as if generated by a voltage controlled oscillator (VCO) or similar circuit.

When Vin is high, that is, Vin is between the values of Vinmax and approximately zero, a current is generated in the drain of device M2. When Vin is negative, that is, Vin has a value between approximately zero and Vinmin, the drain current of device M2 is approximately zero. As waveform 610 increases, the drain current in M2 increases geometrically and reaches a maximum value shown here as I1. The drain current of device M2 is shown as waveform 620, and is graphed as a function of time along X axis [644] 624.

The amplitude of the IF signal provided by the downconverter is detected by RSSI block 940 and presented to the baseband circuit 945. The RSSI block 940 may receive an input from one or both of the outputs of the low pass filters 930 and 932. Alternately, or in combination, the RSSI block may receive an input from one or both of the outputs of the mixers 920 and 925. RSSI block 940 may contain logarithmic amplifiers and rectifiers. Examples of such logarithmic amplifiers can be found in jointly assigned, copending U.S. application number [_____] 09/836,624, filed [_____] April 16, 2001, attorney docket number 20408-001300US, titled "Logarithmic IF Amplifier with Dynamic Large Signal Bias Current, which is hereby incorporated by reference.

1. (Amended) A method of buffering an [RF] input signal comprising:

receiving [an] the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor.